



# JLE05URD4-10A

## 4-Line Ultra Low Capacitance Uni-directional Array

Jialan-Microelectronics

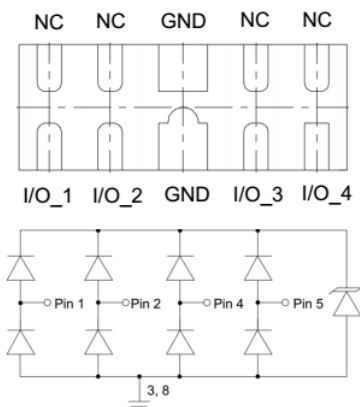
### Description

The JLE05URD4-10A is an ultra low capacitance TVS array, utilizing leading monolithic silicon technology to provide fast response time and low ESD clamping voltage, making this device an ideal solution for protecting voltage sensitive high-speed data lines. The JLE05URD4-10A has an ultra-low capacitance with a typical value at 0.3pF, and complies with the IEC 61000-4-2 (ESD) with  $\pm 15\text{kV}$  air and  $\pm 8\text{kV}$  contact discharge. It is assembled into a 10-pin 2.5x1.0x0.5mm lead-free DFN package. The flow through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines such as USB3.0 and HDMI. The small size, ultra-low capacitance and high ESD surge protection make JLE05URD4-10A an ideal choice to protect HDMI, MDDI, USB 3.0 and other high speed ports.

### Features

- \* Ultra low capacitance: 0.3pF typical(I/O to I/O)
- \* Ultra Low leakage: nA level
- \* Operating voltage: 5V
- \* Low clamping voltage
- \* One power line protects
- \* Complies with following standards:
  - IEC 61000-4-2 (ESD) immunity test
  - Air discharge:  $\pm 15\text{kV}$
  - Contact discharge:  $\pm 8\text{kV}$
  - IEC61000-4-5 (Lightning) 4A (8/20 $\mu\text{s}$ )
- \* RoHS Compliant
- \* Package: DFN2510-10

### Circuit Diagram

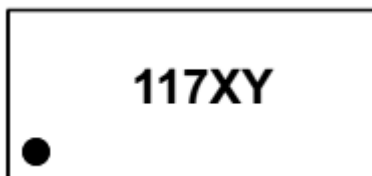


Circuit and Pin Schematic

### Applications

- \* HDMI 1.3 & 1.4, USB 2.0 & 3.0 and MDDI ports
- \* Monitors and flat panel displays
- \* Set-top box and Digital TV
- \* Video graphics cards
- \* Digital Visual Interface(DVI)
- \* Notebook Computers
- \* PCI Express and Serial SATA Ports

### Marking Diagram



#### Transparent top view

117 = Device Code

X = Date Code

Y = Control Code

### Ordering Information

Part Number	Packaging	Reel Size
JLE05URD4-10A	3000/Tape & Reel	7 inch



## JLE05URD4-10A

### Absolute Maximum Ratings ( $T_A=25^{\circ}\text{C}$ unless otherwise specified)

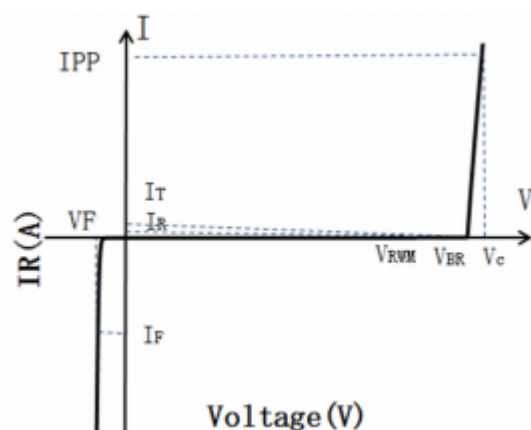
Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20 $\mu\text{s}$ )	Ppk	40	W
Peak Pulse Current (8/20 $\mu\text{s}$ )	IPP	4	A
ESD per IEC 61000-4-2 (Air)	VESD	$\pm 15$	kV
ESD per IEC 61000-4-2 (Contact)		$\pm 8$	
Operating Temperature Range	TJ	-55to +125	$^{\circ}\text{C}$
Storage Temperature Range	Tstg	-55 to +150	$^{\circ}\text{C}$

### Electrical Characteristics ( $T_A=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{\text{RWM}}$	Any I/O pin to ground			5	V
Breakdown Voltage	$V_{\text{BR}}$	$I_{\text{T}} = 0.2\mu\text{A}$ , any I/O pin to ground	5.8			V
Breakdown Voltage	$V_{\text{BR}}$	$I_{\text{T}} = 1\text{mA}$ , any I/O pin to ground		8		V
Reverse Leakage Current	$I_{\text{R}}$	$V_{\text{RWM}} = 5\text{V}$ , any I/O pin to ground			0.5	$\mu\text{A}$
Clamping Voltage	$V_{\text{C}}$	$I_{\text{PP}} = 1\text{A}$ (8 x 20 $\mu\text{s}$ pulse), any I/O pin to ground			9	V
Clamping Voltage	$V_{\text{C}}$	$I_{\text{PP}} = 4\text{A}$ (8 x 20 $\mu\text{s}$ pulse), any I/O pin to ground			10	V
Junction Capacitance	$C_{\text{J}}$	$V_{\text{R}} = 0\text{V}$ , $f = 1\text{MHz}$ , between I/O pins		0.3	0.4	pF
Junction Capacitance	$C_{\text{J}}$	$V_{\text{R}} = 0\text{V}$ , $f = 1\text{MHz}$ , any I/O pin to ground		0.6	0.8	pF

### Portion Electronics Parameter

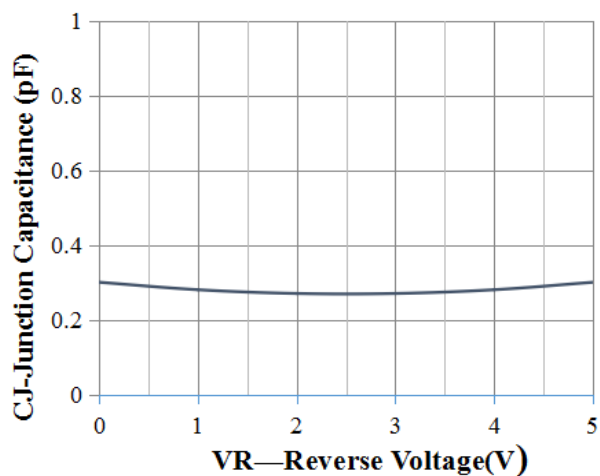
Symbol	Parameter
$I_{\text{T}}$	Test Current
$I_{\text{PP}}$	Maximum Reverse Peak Pulse Current
$V_{\text{C}}$	Clamping Voltage @ $I_{\text{C}}$



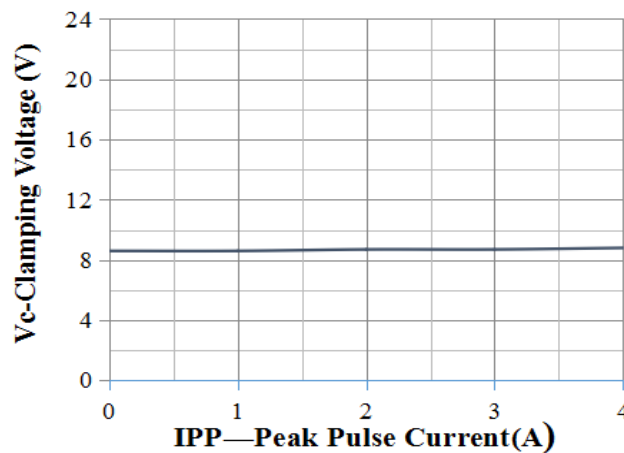


## JLE05URD4-10A

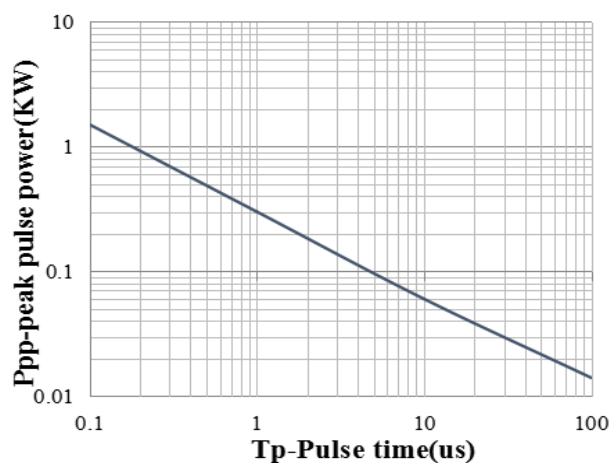
### Typical Performance Characteristics ( $T_A=25^{\circ}\text{C}$ unless otherwise Specified)



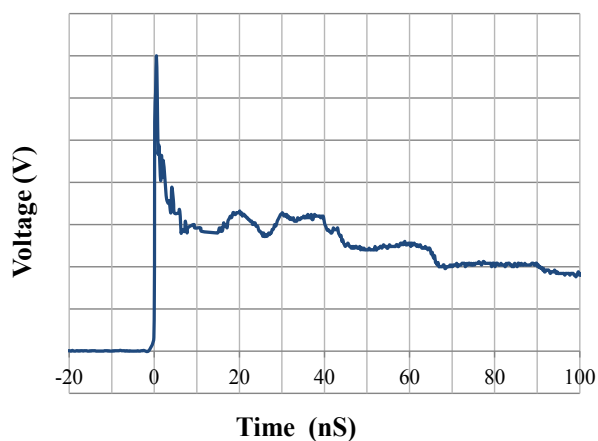
Junction Capacitance vs. Reverse Voltage



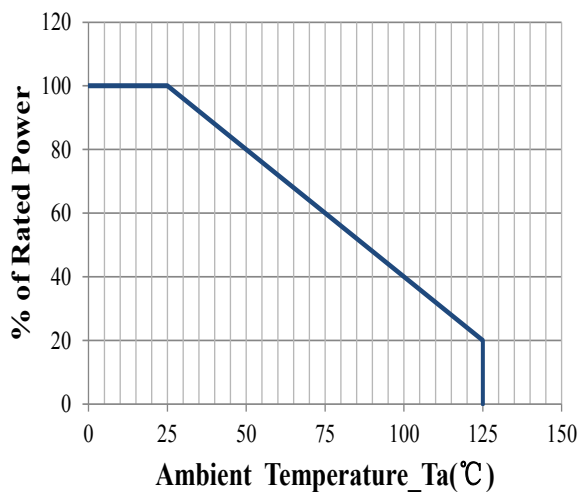
Clamping Voltage vs. Peak Pulse Current



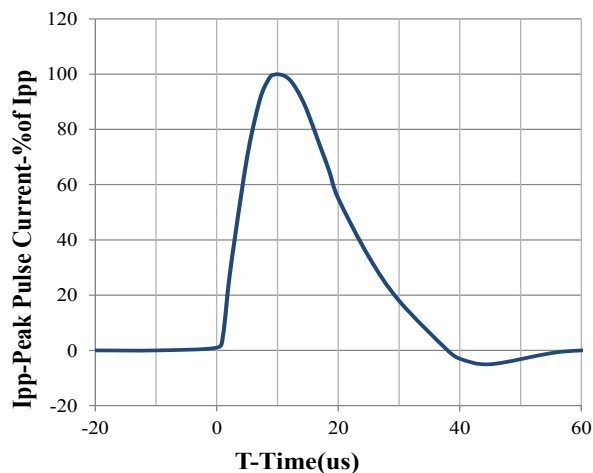
Peak Pulse Power vs. Pulse Time



IEC61000-4-2 Pulse Waveform



Power Derating Curve



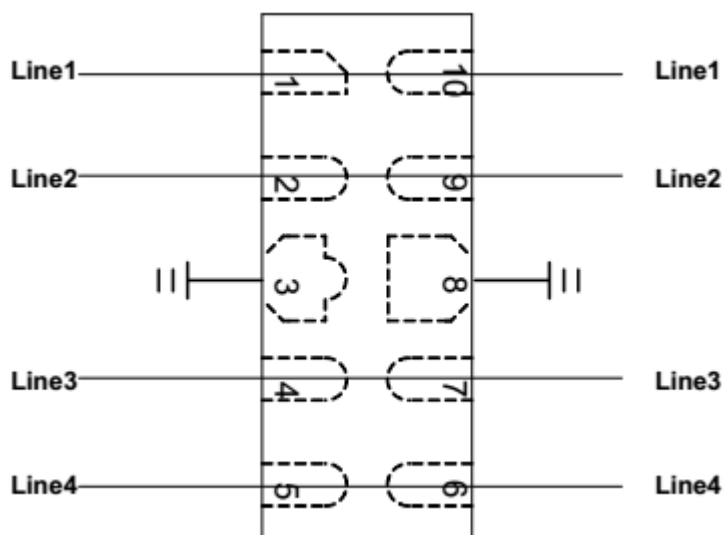
8 X 20us Pulse Waveform



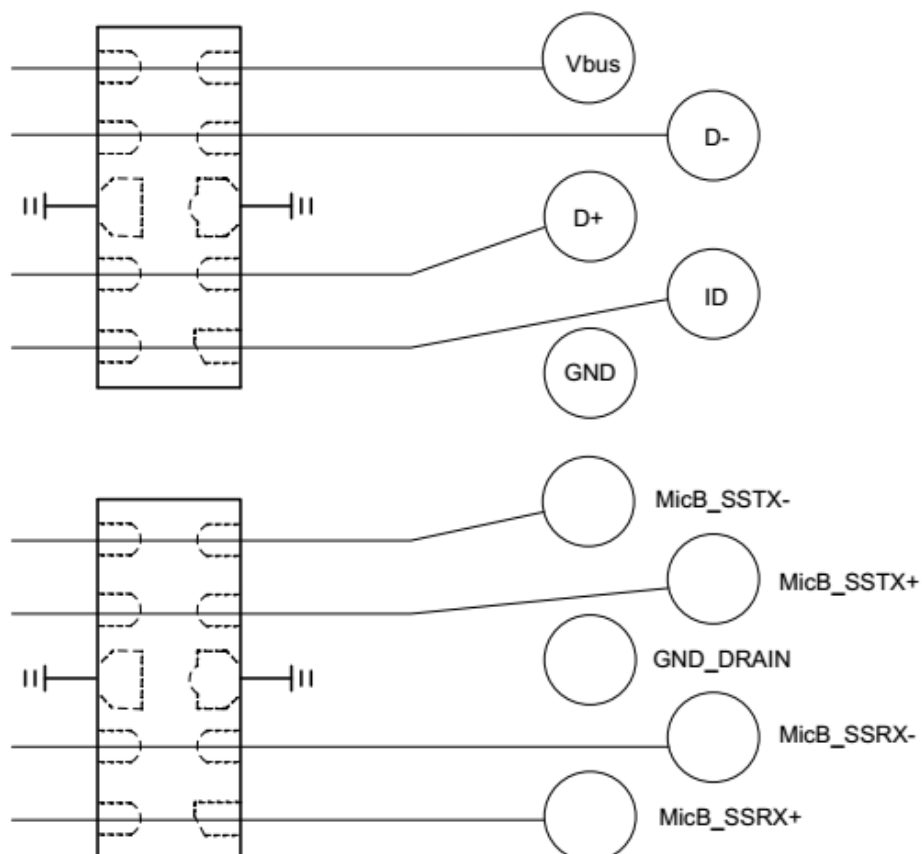
## JLE05URD4-10A

### Typical Application

The JLE05URD4 -10A is designed for easy PCB layout by allowing the traces to run straight through the device. The PCB traces could be used to connect the pin pairs for each line. For example, line 1 enters at pin 1 and exits at pin 10 and the PCB trace connects Pin 1 and Pin 10 together. Ground is connected at Pin 3 and Pin 8.



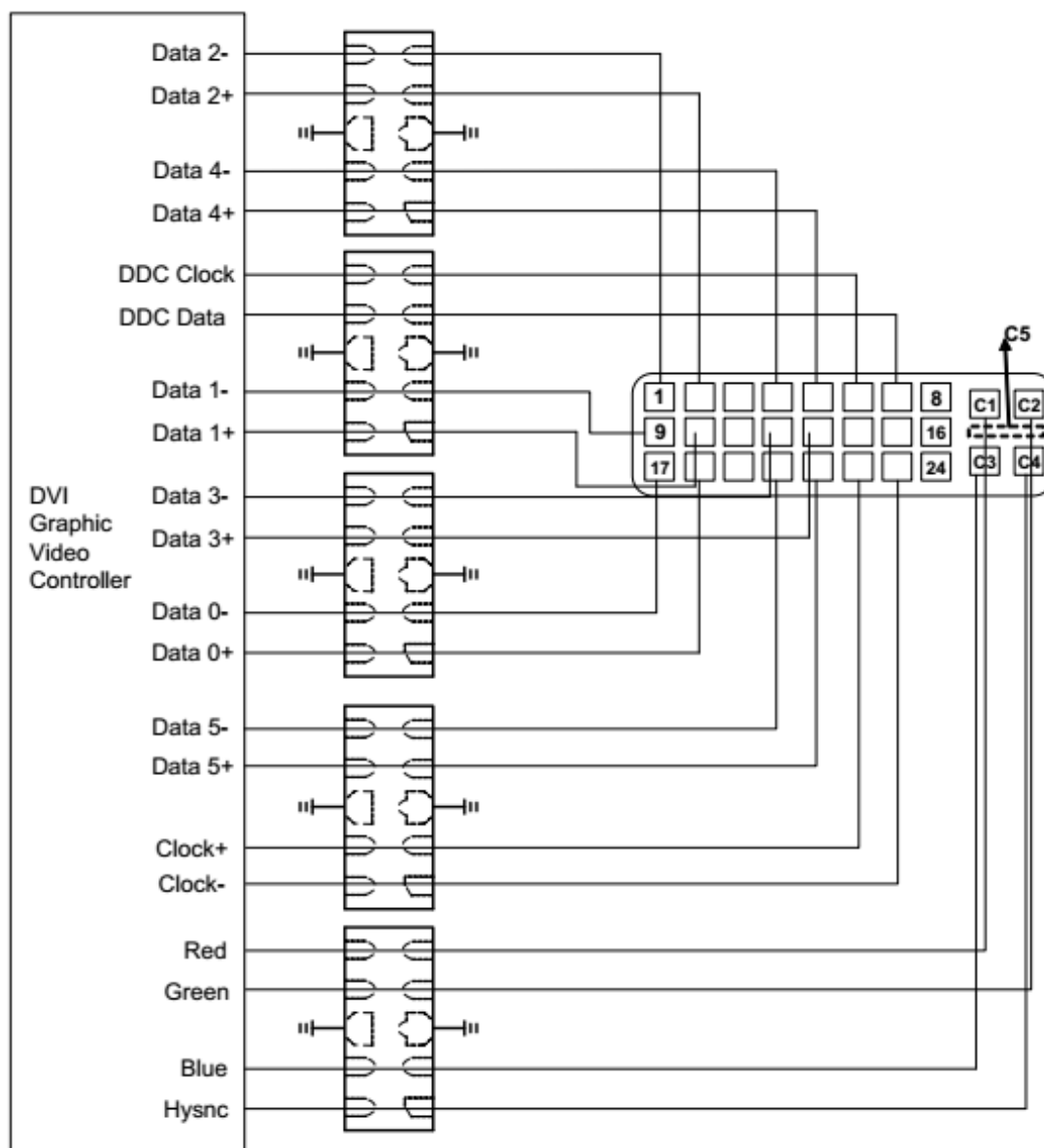
### JLE05URD4-10A On USB 3.0 Port Application





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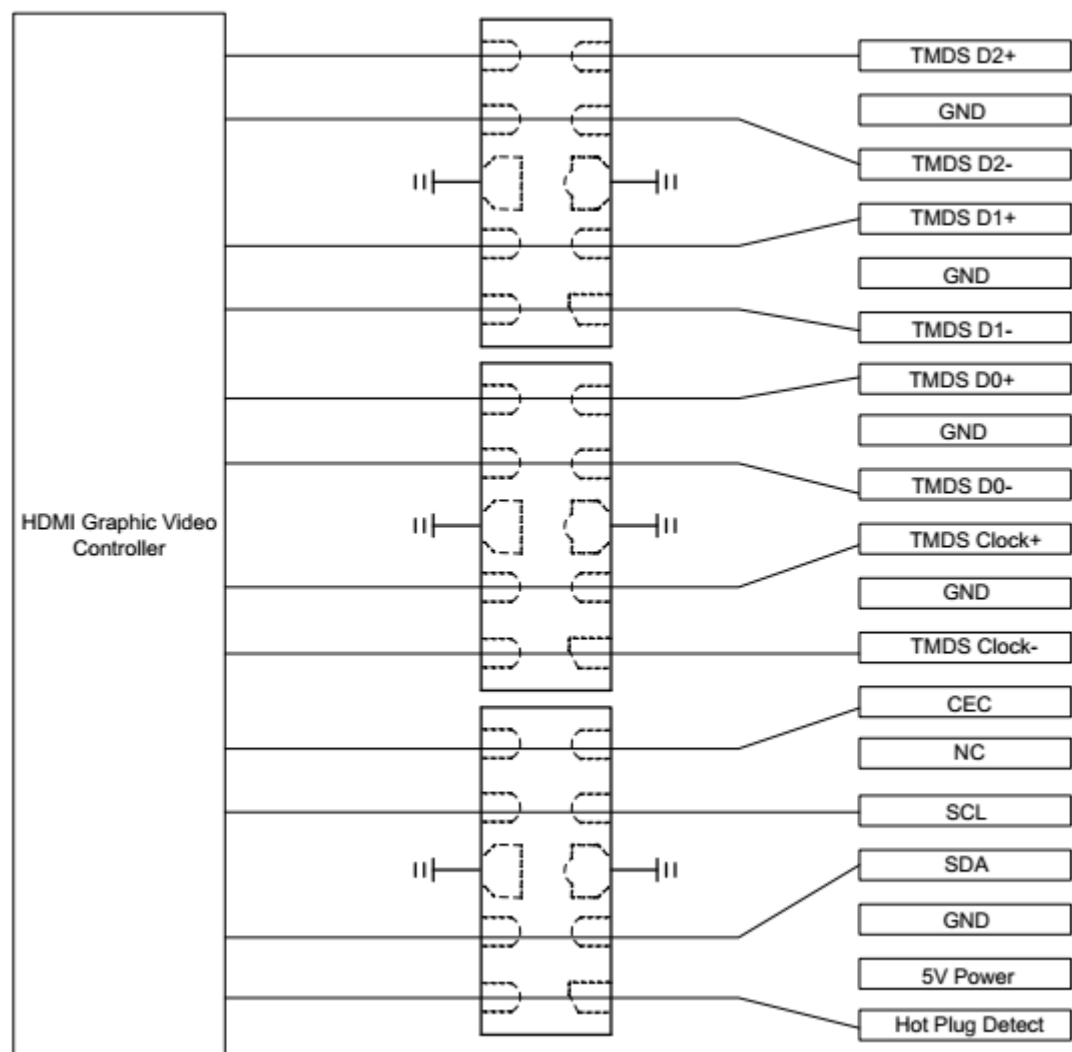
### JLE05URD4-10A On DVI Port Application





## JLE05URD4 -10A

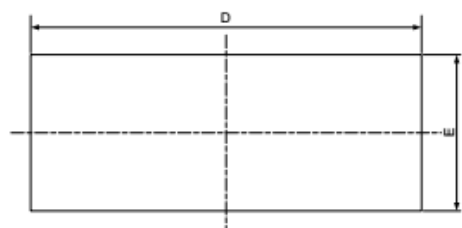
### JLE05URD4 -10A On HDMI Port Application



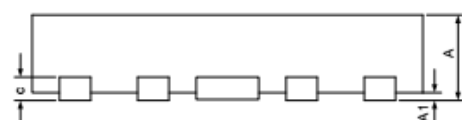


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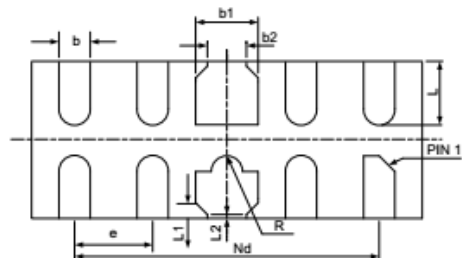
### DFN2520-10 Package Outline Drawing (Dimensions in millimeters)



TOP VIEW



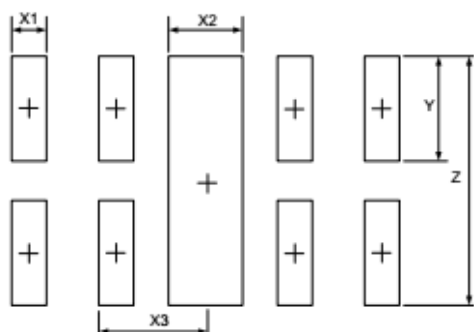
SIDE VIEW



BOTTOM VIEW

SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
b1	0.35	0.40	0.45	0.014	0.016	0.018
b2	0.20	0.25	0.30	0.008	0.010	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.45	2.50	2.55	0.098	0.100	0.102
e	0.50BSC			0.020BSC		
Nd	2.00BSC			0.080BSC		
E	0.95	1.00	1.05	0.038	0.040	0.042
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.075REF			0.003REF		
L2	0.050REF			0.002REF		
h	0.08	0.12	0.15	0.003	0.005	0.006
R	0.05	0.10	0.15	0.002	0.004	0.006

### Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
X1	0.200	0.008
X2	0.400	0.016
X3	0.500	0.020
Y	0.600	0.024
Z	1.400	0.056

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